UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,206	04/01/2004	Paul Wilson	HLZ-013	2441

959 7590 04/23/2007

LAHIVE & COCKFIELD, LLP
ONE POST OFFICE SQUARE
BOSTON, MA 02109-2127

EXAMINER	
PATEL, DHAVAL V	
ART UNIT	**PAPER NUMBER**
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,206	WILSON, PAUL	
	Examiner	Art Unit	
	Dhaval Patel	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,12-14,16 and 17* is/are rejected.

7)☒ Claim(s) *4,8-11,15,18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/7/2004 & 7/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 9/7/2004 and 7/27/2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to because of improper labeling. For example, drawings should label as "Figure 1" (as shown in specification page 4 line 22) instead of "Fig1" (as shown in drawings sheets 1-4). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following minor informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Suggested title would be " PARALLEL MODE EQUALIZER ARCHITECTURE USING DUAL TAPPED DELAY LINES WITH CLOCK AND INVERSE CLOCK SIGNALS".

Appropriate correction is required.

Claim Objections

4. Claim 18 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 18 fails to further limit the parent claim as required under 35 U.S.C 112 4th paragraph. It fails the "Infringement Test". See MPEP 608.01(n).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 discloses the number of N tapped delay lines, wherein N>2, for receiving samples of the input signal in sequence. However, applicant fails to disclose the method of using the disclosed invention with the tapped delay line greater than 2. It does not clearly define in the specification as well as in the drawings, how this equalizer works with the tapped line greater than 2.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5-7, 12-14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizoguchi Shoichi (EP 0379375) (hereafter Mizoguchi)

Regarding claim 1, Mizoguchi teaches an equalizer comprising a first tapped delay line, for receiving samples of an input signal at a first series of time points (abstract, fig. 2, col.4 line 32-46 transversal filter 2 has a tapped delay lines for receiving input signals), a second tapped delay line, for receiving samples of an input signal at a second series of time points, wherein successive time points alternate between the first and second series of time points, (abstract, fig. 2, claim 1,col. 5 line 1-5 Transversal filter 4 has a tapped delay lines), a first summing circuit, for forming a first output as a weighted sum of sample values from a first series of tap points in the first tapped delay line and a first series of tap points in the second tapped delay line, wherein tap points in the first series of tap points in the first tapped delay line are at delays intermediate between the delays of successive tap points in the first series of tap points in the

second tapped delay line (abstract, fig. 2, col. 4 line 43-53), a second summing circuit, for forming a second output as a weighted sum of sample values from a second series of tap points in the first tapped delay line and a second series of tap points in the second tapped delay line, wherein the respective first and second series of tap points each alternate in the first and second tapped delay lines, and wherein tap points in the second series of tap points in the first tapped delay line is at delays intermediate between the delays of successive tap points in the second series of tap points in the second tapped delay line (Abstract, figure 2, claim 1, col. 5 lines 5-9), an output, for forming an equalizer output signal from the first output at a third series of time points, and from the second output at a fourth series of time points, wherein the third and fourth series of time points alternate (Abstract, figure 2, col. 4 lines 43-46, col. 4 lines 53-56, col.5 lines 5-9).

Regarding claim 2, Mizoguchi discloses claim 1, Mizoguchi also teaches an equalizer, wherein the first tapped delay line comprises a first plurality of controllable memory elements (tapped delay line consisting of delay elements or shift registers 31 and 32. col. 4 line 32-35) and the second tapped delay line comprises a second plurality of controllable memory elements (tapped delay line consisting of delay elements or shift registers 31 and 32. col. 5 lines 1-5 discloses another filter with the same structure), each of the controllable memory elements

alternating between time periods in which its output is static and time periods in which its output may be in transition (fig 2, col. 6 lines 8-14).

Regarding claim 3, Mizoguchi discloses claim 1 & 2, Mizoguchi further teaches an equalizer, wherein the controllable memory elements (fig. 2,tapped delay line consisting of delay elements or shift registers 31 and 32. Col.4 line 32-35) are controlled such that the outputs of the first series of tap points in the first tapped delay line and the first series of tap points in the second tapped delay line are static at the third series of time points, and such that the outputs of the second series of tap points in the first tapped delay line and the second series of tap points in the second tapped delay line are static at the fourth series of time points (fig. 2,3 col. 7, line 34-47, fig. 2,3).

Regarding claim 5, Mizoguchi discloses claim 1, Mizoguchi further teaches an equalizer as claimed in claim 1 comprising: a number N of tapped delay lines, wherein $N > 2$ (abstract, figure 4A, 4b, as shown has more than 2 transversal filter connected with input signal and has more than 2 tapped delay lines, col. 3, Line 45-50,col.7 line 56-59), for receiving samples of the input signal in sequence, a number N of summing circuits (fig. 4A, 4B as shown has more than 2 summing circuits), for forming respective outputs as weighted sums of sample values from a respective series of points arranged sequentially in the tapped delay lines, an

output, for forming the equalizer output signal from the outputs of the summing circuits sequentially (fig. 4A, 4B as shown has more than 2 summing circuits for the three tapped delay line transversal filters).

Regarding claim 6, Mizoguchi discloses claim 1, Mizoguchi also teaches an equalizer, wherein the first tapped delay line comprises a first series of analog track and hold circuits (Tapped delay line consisting of unit delay elements or shift registers 31 and 31, see col. 4, line 32-34, also figure 2 has a Latch 37 is connected to the successive tapped delay lines, which is one kind of memory elements, col. 4 line 48-50), and the second tapped delay line comprises a second series of analog track and hold circuits (fig 2 has a Latch 37 is connected to the successive tapped delay lines, which is one kind of memory elements, col. 4 line 48-50 wherein Tapped delay line consisting of unit delay elements or shift registers 31 and 31, see col. 4, line 32-34).

Regarding claim 7, Mizoguchi discloses claim 1, Mizoguchi also teaches an equalizer, wherein the first tapped delay line comprises a first series of digital sample and hold circuits, and the second tapped delay line comprises a second series of digital sample and hold circuits (abstract defines that each transversal filter symbol appearing at successive tapes of tapped-delay line are sampled and held for a duration of N symbols).

Regarding claim 12, Mizoguchi teaches an equalizer comprising a plurality of tapped delay lines, for receiving received sample values in sequence, and a corresponding plurality of summing circuits, such that an output signal is formed from an output of each of the plurality of summing circuits in sequence (abstract, fig 1,2,4a, 4b, col.2 line 44-51).

Regarding claim 13, Mizoguchi discloses an equalizer, comprising: an input, for demultiplexing alternate samples of a received signal into first and second data streams; a first tapped delay line (fig 2, col. 4 lines 24-31 discloses that output of A/D converter is applied to input of the tapped delay line of first filter and on the other hand one symbol delay line to the input of the tapped delay line of other filter), connected to receive the first data stream, and comprising a first plurality of controllable memory elements (fig 2 shows tapped delay line consisting of delay elements or shift registers 31 and 32. col.4 line 32-35); a second tapped delay line, connected to receive the second data stream, and comprising a second plurality of controllable memory elements (fig. 2,tapped delay line consisting of delay elements or shift registers 31 and 32. Col. 5, lines 1-5); and an output, wherein each of the controllable memory elements alternates between time periods in which its output is static and time periods in which its output may be in transition (fig 2, col. 6 lines 8-14), wherein the controllable memory elements

in the first tapped delay line are alternately members of a first group of controllable memory elements whose outputs are static during first time periods and may be in transition during second time periods, alternating with the first time periods, and a second group of controllable memory elements whose outputs are static during second time periods and may be in transition during first time periods (fig 2, col. 6 lines 8-12 defines that delayed clock frequency is in opposite in phase to the non delayed lower frequency clock), wherein the controllable memory elements in the second tapped delay line are alternately members of a third group of controllable memory elements whose outputs may be in transition during first time periods and are static during second time periods (fig 2, col. 6 lines 8-12 clearly defines that delayed clock frequency is in opposite in phase to the non delayed lower frequency clock), and a fourth group of controllable memory elements whose outputs are static during first time periods and may be in transition during second time periods (fig 2, col. 6 lines 8-12 defines that delayed clock frequency is in opposite in phase to the non delayed lower frequency clock) and wherein the output receives a weighted sum of the outputs of the controllable memory elements of the first and fourth groups during first time periods, and receives a weighted sum of the outputs of the controllable memory elements of the second and third groups during second

time periods (fig 2, col. 6 lines 8-12 defines that delayed clock frequency is in opposite in phase to the non delayed lower frequency clock).

Regarding claim 14, Mizoguchi discloses claim 13, Mizoguchi also teaches an equalizer, wherein the output comprises a first summing circuit for forming the weighted sum of the outputs (fig 2, col. 4 lines 43-60, Also, it is clear in the abstract that it has a N successive tapped delay lines) of the controllable memory elements (fig 2, col. 4 line 32-35) of the first and fourth groups and a second summing circuit for forming the weighted sum of the outputs periods (fig. 2, col. 5 line 1-9,) of the controllable memory elements (fig 2, col. 4 line 32-35) of the second and third groups, and wherein the output is adapted to supply the output of the first summing circuit as an output during first time periods and to supply the output of the second summing circuit as an output during second time (abstract, figure 2, col. 4 lines 43-46, col. 4 lines 53-55, col. 5 lines 5-9).

Regarding claim 16, Mizoguchi discloses claim 13, Mizoguchi also teaches an equalizer, wherein the controllable memory elements comprise analog track and hold circuits (fig 2, col. 4 line 32-35, col. 4 line 48-58 also discloses latch which is a also a memory elements to track and hold symbols driven by the clock cycle).

Regarding claim 17, Mizoguchi discloses claim 13, Mizoguchi also teaches an equalizer as claimed in claim 13, wherein the controllable memory elements

comprise digital track and hold circuits. (fig. 2, col. 4 line 32-35, col. 4 lines 48-58 also discloses latch, which is also a memory elements to track and hold symbols driven by the clock cycle).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizoguchi.

Mizoguchi fails to explicitly disclose an optical receiver for converting an optical signal into an electrical signal for use in an Equalizer as claimed. However, examiner takes Official Notice that such aspect is very well known and used in the art for wideband signal processing. Therefore, it would have been obvious for one skilled in the art to utilize optical receiver in conjunction with equalizer for wideband signal processing.

Allowable Subject Matter

8. Claims 4, 8-11 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claims 4, 8-11 and 15 are allowed because the references cited failed to teach, an applicant has, an equalizer, wherein the first tapped delay line comprises a first plurality of track and hold circuits, and the second tapped delay line comprises a second plurality of track and hold circuits, and wherein track and hold circuits preceding the first series of tap points in the first tapped delay line and track and hold circuits preceding the first series of tap points in the second tapped delay line are clocked by a first clock signal, track and hold circuits preceding the second series of tap points in the first tapped delay line and track and hold circuits preceding the second series of tap points in the second tapped delay line are clocked by a second clock signal, wherein the second clock signal is the inverse of the first clock signal. An equalizer, in the form of a decision feedback equalizer with decision circuits for forming first and second binary outputs from the first and second outputs, a second part of said first tapped delay line, for receiving the first binary output as an input thereto, a second part of said second

tapped delay line, for receiving the second binary output as an input thereto, wherein the first summing circuit forms the first output as a weighted sum of sample values from a first series of alternate points in the first tapped delay line including the second part of said first tapped delay line and a first series of alternate points in the second tapped delay line including the second part of said second tapped delay line, and wherein the second summing circuit forms the second output as a weighted sum of sample values from a second series of alternate tap points in the first tapped delay line including the second part of said first tapped delay line and a second series of alternate tap points in the second tapped delay line including the second part of said second tapped delay line. An equalizer, wherein the first tapped delay line comprises a first plurality of controllable memory elements, and the second tapped delay line comprises a second plurality of controllable memory elements, each of the controllable memory elements alternating between time periods in which its output is static and time periods in which its output may be in transition. An equalizer, wherein the controllable memory elements are controlled such that the outputs of the first series of tap points in the first tapped delay line and the first series of tap points in the second tapped delay line are static at the third series of time points, and such that the outputs of the second series of tap points in the first tapped delay line and the

second series of tap points in the second tapped delay line are static at the fourth series of time points. An equalizer, wherein the first tapped delay line comprises a first plurality of track and hold circuits, and the second tapped delay line comprises a second plurality of track and hold circuits, and wherein track and hold circuits preceding the first series of tap points in the first tapped delay line and track and hold circuits preceding the first series of tap points in the second tapped delay line are clocked by a first clock signal, track and hold circuits preceding the second series of tap points in the first tapped delay line and track and hold circuits preceding the second series of tap points in the second tapped delay line are clocked by a second clock signal, wherein the second clock signal is the inverse of the first clock signal. An equalizer comprising means for supplying a clock signal to the controllable memory elements of the first and fourth groups, and for supplying an inverted clock to the controllable memory elements of the second and third groups, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled " Comments on Statement of Reasons for allowance."

Conclusion

The corresponding US Patent for the EP 0379375 is US 5005585 A.

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patel Dhaval whose telephone number is (571) 270-1818. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571) 272-7332. Customer Service can be reached at (571) 272-2600. The fax number for the organization where this application or proceeding is assigned is (571) 273-7332.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dhaval Patel

4/4/2007

VU LE
SUPERVISORY PATENT EXAMINER